A 30 GHz - 100 mW GaAs FET

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ABSTRACT

Power output of 100 mW and linear power gain of 5 dB have been realized at 30 GHz for the GaAs FET fabricated by optimizing physical parameters of the channel for high power end.

Introduction

During the past few years, GaAs FETs fabricated by electron beam lithography have demonstrated their excellent low noise and small signal gain performances as high in frequency as in Ka-band.(1),(2) Microwave systems in Ka-band, however, require high power GaAs FETs as well, which are expected to replace IMPATT diodes used in a transmission amplifier in 30/20 GHz satellite communication band. Inadequately examined, at present, is the question how high in power the GaAs FETs will provide in Ka-band.

The experimental results presented here will prove that the GaAs FETs having power output of 100 mW with 5 dB linear power gain are obtained.

Device Fabrication

Though electron-beam lithography will be very useful to fabricate the GaAs FET with submicron gate length, some basic design considerations for obtaining high power performance in Ka-band were investigated here with ordinary photo-lithographical technique. In short, a high power version of the low noise GaAs FET presented earlier as MGF-1403 (3) was developed by optimizing physical parameters of the channel to obtain higher drain current and breakdown voltage. Typically, channel doping was 2.0×10^{17} cm^{-3} and channel thickness before gate recess was as thick as 0.5 μm. The ohmic contacts for drain and source were Au-Ge-Ni alloy and gate metal was Al. Each electrode has a Cr-Mo-Au overlay metal layer for bonding purpose. The surface of the GaAs FET chip was coated with Si_3N_4. Figure 1 shows a photograph of the chip surface. Typical gate length was 0.6 μm which was ascertained by SEM observation. Length of each gate finger is 75 μm and total gate width is 300 μm. By adjusting the channel thickness under the gate, drain currents around 100 mA were obtained with breakdown voltage over 15 V, which was high enough for the FET operating with drain bias at 8 V.

Circuit Description

The GaAs FET was bonded, as shown in Fig.2, on a chip carrier constructed with 0.635 mm or 0.38 mm thick alumina substrates and was incorporated into a mount described below for measuring power performance. The input-output power performance was measured using the mount whose inside view is shown in Fig.3. WRJ-320 waveguides were adopted for input and output port connections. Adjacent to input and output edges of the FET chip carrier were inserted microstrip circuit which include an interdigitated dc blocking capacitor and a rf choke for dc biasing. The microstrip circuit was converted through a ridge-line transformer to the waveguide with a slide screw tuner, which serves to compensate mismatching incidental to conversion. Replacing the chip carrier with a straight microstrip line, transmission loss of the mount was measured and 1.2 dB insertion loss was obtained at 29-31 GHz.

Performance of GaAs FET

In the measurement of the input-output power performance of the GaAs FETs, some microstrip circuits or metal slugs were formed on the chip carrier for better matching. Slide screw tuners in the waveguide were used for additional fine adjustment. Figure 4 shows an example of the input-output power performance. Power output of 100 mW is obtained with 2dB power gain and with linear power gain of 5 dB. Figure 5 and Fig.6 show distribution of saturation power (P_{sat}) and linear power gain (G_L) for the GaAs FETs randomely picked up out of 7 different lots. These results demonstrate that power output of 100 mW is surely realizable.

Amplifier Performance

As the first step of developing medium power amplifiers, small signal amplifiers were studied.

Using S-parameters of the GaAs FET chip, matching networks were designed and incorporated into an amplifier. Figure 7 shows input and output impedance loci between 28.5 and 30.5 GHz. As shown in Fig.8, about 4 dB of power gain is obtained from 28.5 to 29.5 GHz and peak power gain is 5 dB at 28.7 GHz. This measurement was carried out by using only the matching networks mentioned above and the slide screw tuners were not used. Figure 9 shows an input-output power performance of a cascaded amplifier composed of two amplifiers mentioned above. A linear power gain of 11.8 dB was obtained at 28.6 GHz.

Conclusion

By optimizing physical parameters of the channel, power output of 100 mW was realized at 30 GHz. An amplifier has linear power gain of 4 dB in a frequency range 28.5-29.5 GHz. A cascaded amplifier showed 11.8 dB of linear power gain at 28.6 GHz.

0149-645X/81/0000-0325$00.75

Acknowledgement

The authors wish to express their appreciation to T.Suzuki for his helpful technical advice, to M.Yabe and T.Nakazawa for their helpful discussions in circuit design and mesurements.

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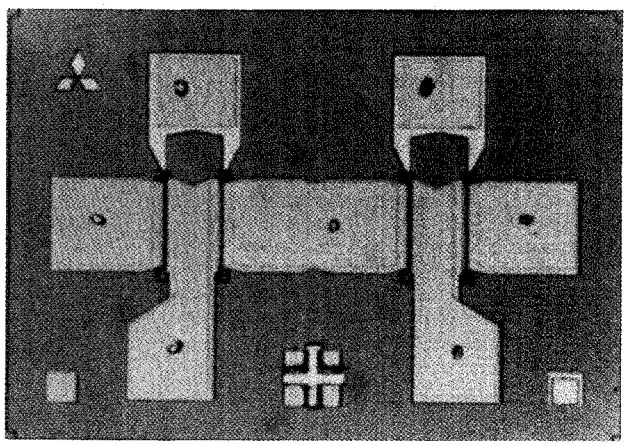


Fig. 1 Microphotograph of GaAs FET.

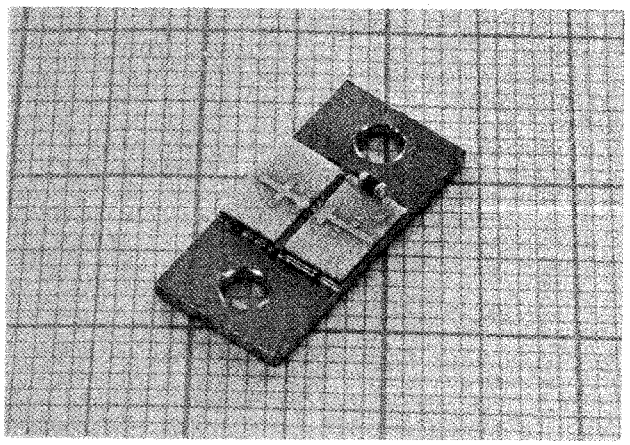


Fig.2 Photograph of chip carrier.

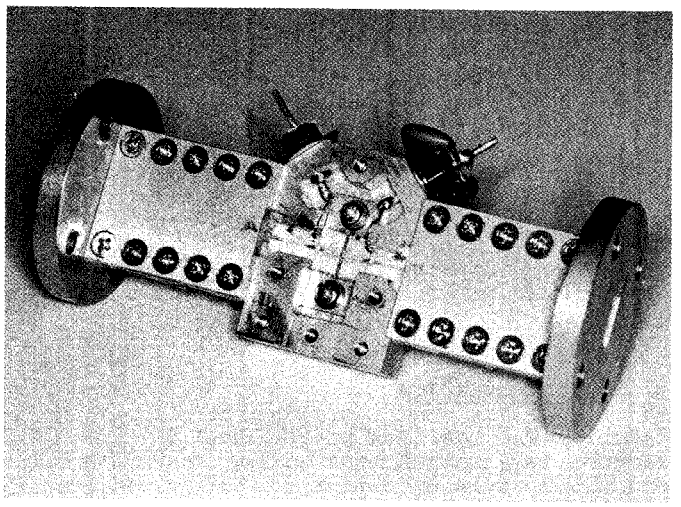


Fig.3 Inside view of test mount.

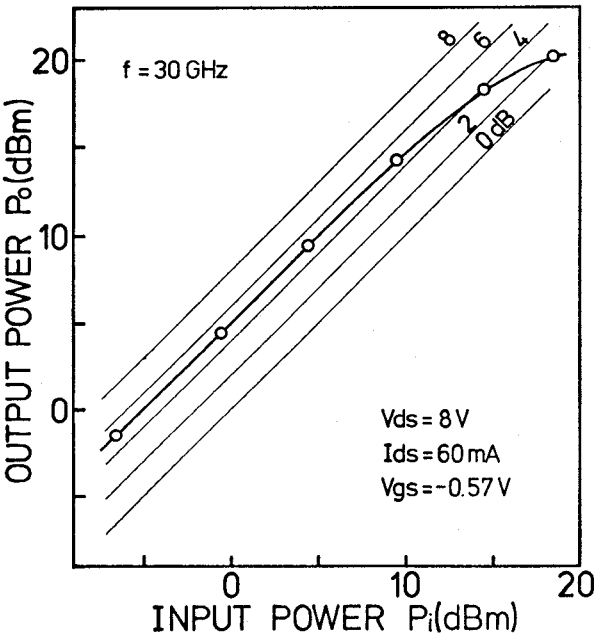


Fig.4 Input-output power performance of developed GaAs FET.

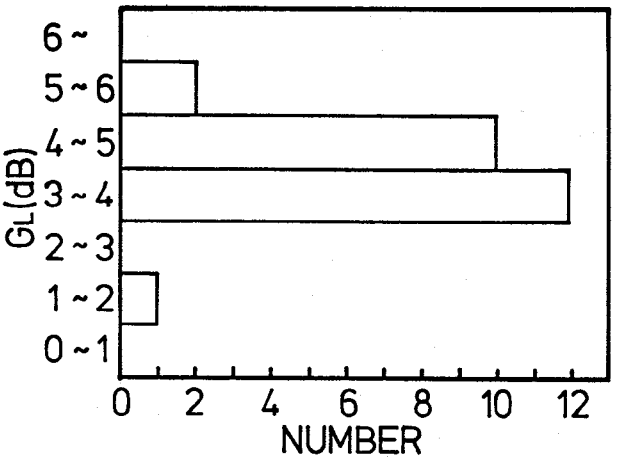


Fig.5 Distribution of linear power gain.

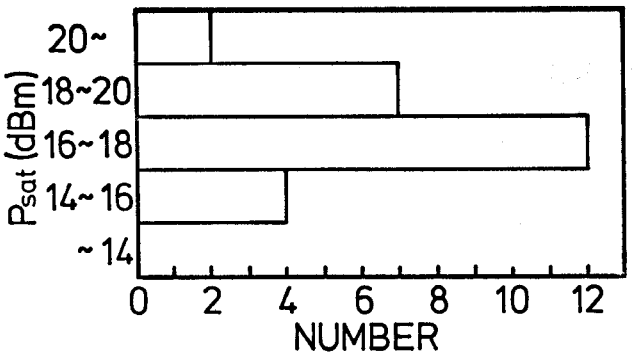


Fig.6 Distribution of saturation power.

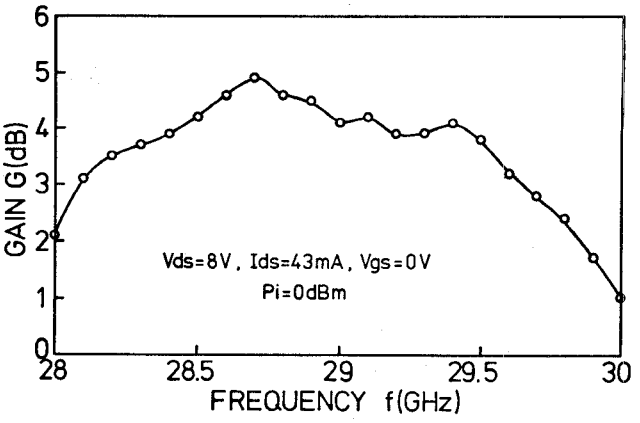
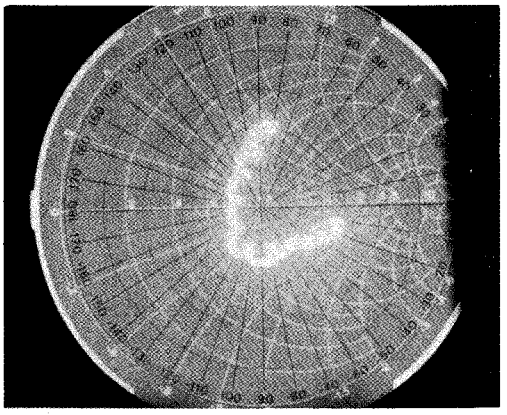
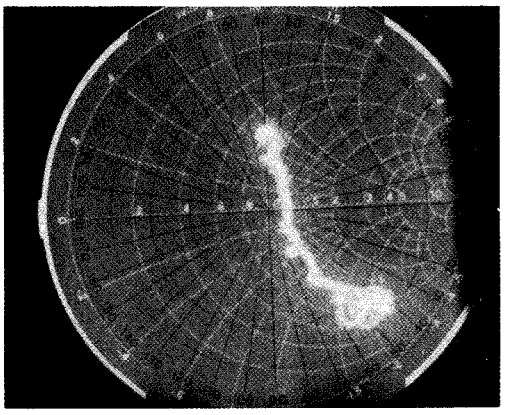


Fig.8 Amplifier performance without slide screw tuners.



(a)



(b)

Fig.7 Input (a) and output (b) impedance loci of an amplifier.

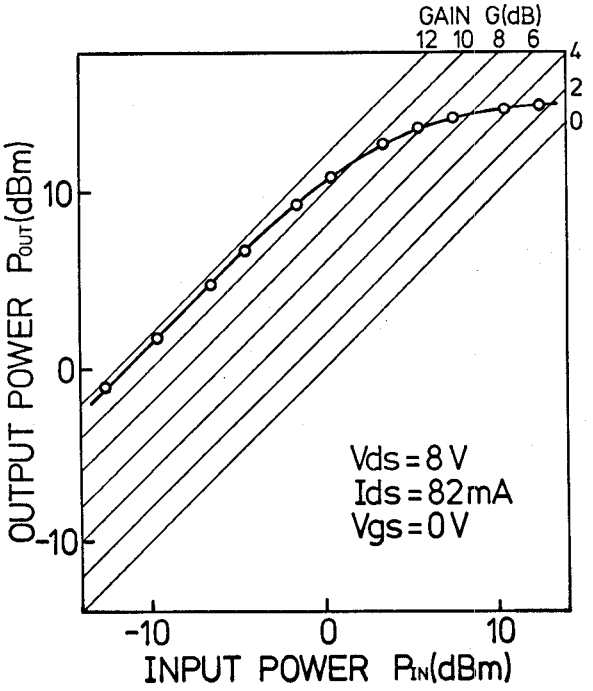


Fig.9 Input-output power performance of cascaded amplifier.